

MITSUBISHI LSIs

M5C6847P-1

VIDEO DISPLAY GENERATOR

DESCRIPTION

The M5C6847P-1 is a color or monochrome television interface device, fabricated using N-channel silicon gate ED-MOS technology.

The M5C6847P-1 has a 64-character (6-bit ASCII code) generator and memory interface.

FEATURES

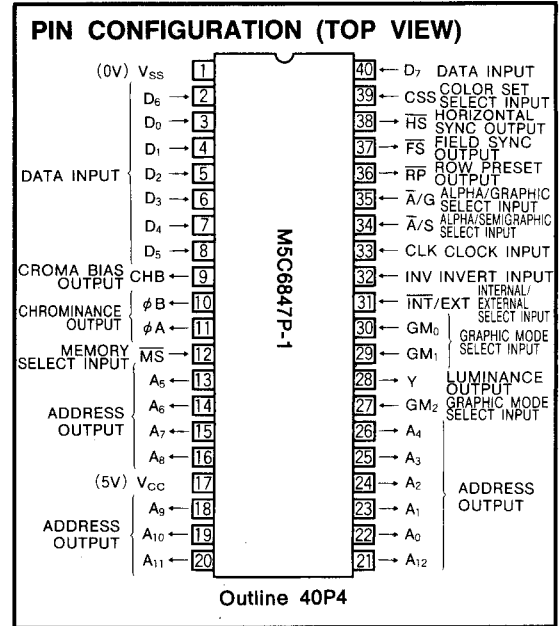
- Can be easily connected to the MELPS 85 series 8-bit CPUs.
- Alphanumeric display: 4 modes
- Graphic display: 8 modes
- Can connect directly with M51342P RF modulator
- Alphanumeric display: 32 characters per line by 16 lines
- Character generator for 64 ASCII characters
- Can be used with an external character generator
- Generates composite video signals
- Generates intensity signal Y, color signal R-Y (ϕA) and B-Y (ϕB)
- Display RAM capacity (depends on mode): 512 ~ 6K bytes
- Single 5V power supply

APPLICATION

Microcomputer system or terminals using a color or monochrome CRT.

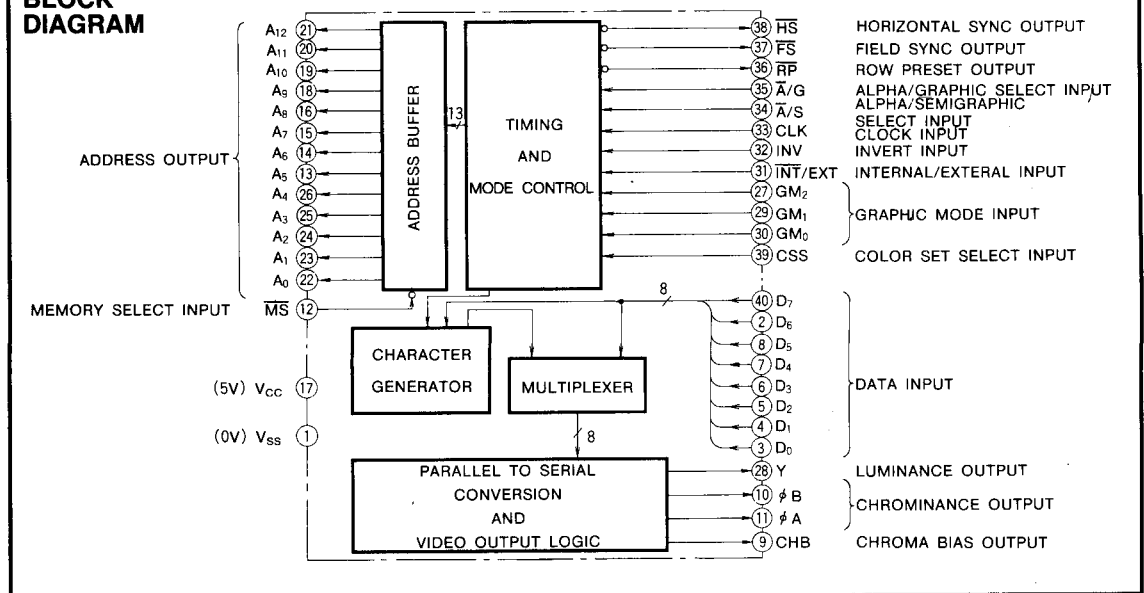
FUNCTION

The picture on the television set is composed of the synchronization signals such as horizontal synchronization signal, vertical synchronization signal and color burst signal, and synchronizing serial data. M5C6847P-1 can generate



these signals. The information or data to be shown on the screen is written in the display memory by the CPU. (When the picture is to be composed on a CRT) the data for one screen in the display memory is read in the order of the scan cycles and synchronization signals are added. This serial is sent to the RF modulator. The M5C6847P-1 performs these functions by reading the display memory in the order of the CRT scan, adding the required synchronization signals such as luminance signal, color signal and then transferring

BLOCK DIAGRAM



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the data stream serially to the RF modulator.

OPERATION

Data Input (D₇~D₀)

Eight TTL-compatible data lines are used to input data from the display memory to be processed by the M5C6847P-1. The data is interpreted and transformed into video analog level signals.

Address Outputs (A₁₂~A₀)

Thirteen address lines are used by the M5C6847P-1 to access the display memory (refresh memory). The starting address of the display memory is located at the upper-left corner of the display screen. As the television sweeps from the left to right and top to bottom, the VDG increments the RAM display address. The address lines are TTL-compatible and may be forced in a high-impedance state when input \overline{MS} goes low.

Video Output (Y, ϕ_A , ϕ_B ,)

These video outputs are used to transfer luminance and color information of pictures displayed on television with standard NTSC systems. These outputs can be directly connected to the RF modulator M51342P.

Chrominance Output (ϕ_B)

The chrominance output ϕ_B is a 4-level analog output. These levels of the signal are used in combination with ϕ_A and Y to specify one of eight colors. The other level is used to specify the time of the color burst reference signal.

Chrominance Output (ϕ_A)

The chrominance output ϕ_A is a 3-level analog output. The signal is used in combination with ϕ_B and Y to specify one of eight colors.

Chroma Bias Output (CHB)

The chroma bias output is a single level analog output that provides the DC reference for chrominance outputs.

Luminance Output (Y)

The luminance output is a 6-level analog output. The six level analog outputs contain composite, blank, and four levels of video intensity.

Synchronization Input (\overline{MS} , CLK)

Memory Select Input (\overline{MS})

This is a TTL compatible input. When it goes low-level, address outputs (A₁₂~A₀) are forced in high-impedance state. When other devices such as the CPU access the display memory, it must be kept at low-level to prevent interference.

Clock input (CLK)

The clock input requires a 3.579545 MHz clock with a duty cycle of 50±5%. The M51342P RF modulator may be used to supply the 3.579545 MHz clock.

Synchronization output (FS, HS, \overline{RP})

The synchronization outputs FS, HS and \overline{RP} are TTL-compatible and provide circuits, exterior to the M5C6847P-1 states.

Row preset output (\overline{RP})

This signal can be used when an external character generator ROM that is used with the VDG. An external 4-bit binary counter must also be added to supply row selection.

The counter is clocked by the HS signal and cleared by the RP signal. See Table 4 ② for details.

Table 1 Operation modes

A/G	A/S	INT	EXT	INV	GM ₀	GM ₁	GM ₂	Mode
0	0	0	0	0	X	X	X	Internal alphanumerics
0	0	0	1	0	X	X	X	Internal alphanumerics inverted
0	0	1	0	0	X	X	X	External alphanumerics
0	0	1	1	0	X	X	X	External alphanumerics inverted
0	1	0	0	X	X	X	X	Semigraphics 4
0	1	1	0	X	X	X	X	Semigraphics 6
1	X	X	X	0	0	0	0	64× 64 Color graphics
1	X	X	X	1	0	0	0	128× 64 Graphics
1	X	X	X	0	1	0	0	128× 64 Color graphics
1	X	X	X	1	1	0	0	128× 96 Graphics
1	X	X	X	0	0	1	0	128× 96 Color graphics
1	X	X	X	1	0	1	0	128×192 Graphics
1	X	X	X	0	1	1	0	128×192 Color graphics
1	X	X	X	1	1	1	1	256×192 Graphics

Note 1 : X is "don't care" bit.

Table 2 Alphanumeric mode display memory, color and display element





Mode	Memory capacity (bits)	Color	Display elements
Internal alphanumerics	521×8	2	 Character is 5×7 dots 12 dots
External alphanumerics	512×8	2	 8 dots 12 dots
Semigraphics 4	512×8	8	 Elements 64×32
Semigraphics 6	512×8	4	 Elements 64×48

Table 3 Graphic mode display memory, color and display element

Mode	Memory capacity (bits)	Color	Display elements
64× 64 Color graphics	1K×8	4	64×64
128× 64 Graphics	1K×8	2	128×64
128× 64 Color graphics	2K×8	4	
128× 96 Graphics	2K×8	2	128×96
128× 96 Color graphics	3K×8	4	
128×192 Graphics	3K×8	2	128×192
128×192 Color graphics	6K×8	4	
256×192 Graphics	6K×8	2	256×192

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Field synchronization output (\overline{FS})

The high to low transition of the \overline{FS} output coincides with the end of active display area. The low to high transition of \overline{FS} coincides with the trailing edge of the vertical synchronization pulse. The CPU should access display memory while \overline{FS} is at low-level to avoid undesired flicker on the screen.

Horizontal synchronization output (\overline{HS})

This signal is used for horizontal synchronization on the CRT. A fall from high-level to low-level indicates the leading edge of the horizontal synchronization signal.

Mode Control Inputs ($\overline{A/G}$, $\overline{A/S}$, $\overline{INT/EXT}$, GM_2 , GM_1 , GM_0 , CSS and INV)

These eight TTL-compatible input signals are used to determine and control the operational modes of the M5C6847P-1. Outline and details of the operational modes are shown in Table 1~3.

Alphanumeric mode

A screen in the alphanumeric mode is composed of 32 characters x 16 lines. Each character occupies space equivalent to an 8 x 12 dot matrix. The internal character generator can generate 64 characters (6-bit ASCII). Each character is formed by a 5 x 7 dot matrix. The low-order 6 bits of the 8-bit data input are used to select 1 of 64 characters and the remaining 2 bits can be used to implement the CSS and INV signal input. Operation in this mode requires a display memory of at least 512 bytes.

Semigraphic 4 mode

A screen in the semigraphics 4 mode is composed of 64 x 32 display elements. A display element is a 4 x 6 dot matrix; that is to say, each 8 x 12 character dot matrix is split into 4 display elements, each display element being a 4 x 6 dot matrix. The low-order 4 bits of the 8-bit data input correspond to the 4 display elements of a character. Three data bits of the remaining 4 bits may be used to select one of eight colors for the entire character box. The extra bit is available to switch the operation mode. Operation in this mode requires a display memory of at least 512 bytes.

Semigraphics 6 mode

A screen in the semigraphics 6 mode is composed of 64 x 48 display elements. A display element is a 4 x 4 dot matrix; that is to say, each 8 x 12 character dot matrix is split into 6 display elements, each display element being a 4 x 4 dot matrix. The low-order 6 bits of the 8-bit data input to the 6 display elements of a character and the remaining 2 bits are used to determine color. Operation in this mode requires a display memory of at least 512 bytes.

Full Graphic Modes

There are 8 full graphic modes. The border color (green or white) is selected by the level of the CSS signal. The CSS pin selects one of two sets of four colors in the four color graphic modes.

Color Graphic Mode 64 x 64

A screen in the 64 x 64 color graphic mode is composed of

64 x 64 display elements. Each display element can be 1 of 4 colors. Operation in this mode requires a display memory of at least 1024 bytes.

Graphic mode 128 x 64

A screen in the 128 x 64 graphic mode is composed of 128 x 64 display elements. Each display element can be green or white depending on the level of the CSS signal. Operation in this mode requires a display memory of at least 1024 bytes.

Color graphic mode 128 x 64

A screen in the 128 x 64 color graphic mode is composed of 128 x 64 display elements. Each display element can be 1 of 4 colors. Operation in this mode requires a display memory of at least 2048 bytes.

Graphic mode 128 x 96

A screen in the 128 x 96 graphic mode is composed of 128 x 96 picture elements. Each display element can be green or white depending on the level of the CSS signal. Operation in this mode requires a display memory of at least 2048 bytes.

Color graphic mode 128 x 96

A screen in the 128 x 96 color graphic mode is composed of 128 x 96 display elements. Each display element can be 1 of 4 colors. Operation in this mode requires a display memory of at least 3072 bytes.

Graphic mode 128 x 192

A screen in the 128 x 192 graphic mode is composed of 128 x 192 display element. Each display element can be green or white depending on the level of the CSS signal. Operation in this mode requires a display memory of at least 3072 bytes.

Color graphic mode 128 x 192

A screen in the 128 x 192 color graphic mode is composed of 128 x 192 display elements. Each picture element can be 1 of 4 colors. Operation in this mode requires a display memory of at least 6144 bytes.

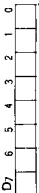




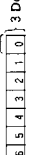

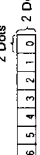
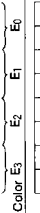
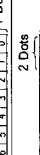
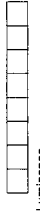
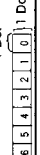
Graphic mode 256 x 192

A screen in the 256 x 192 graphic mode is composed of 256 x 192 display elements. Each display element can be green or white depending on the level of the CSS signal. Operation in this mode requires a display memory of at least 6144 bytes.

Details of the 8 graphic modes are shown in Table 4 which gives more information in an easy to understand form.

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Table 4 Operational characteristics in the various graphic modes

MS	A/G	I/S	Input Pin			Color			TV Screen (1 screen is composed of 256x192 dots)		Display Elements	Data Bus	Display Mode
			INT/EXT	GM ₂	GM ₁	GM ₀	CSS	INV	Character Color	Background			
①	1	0	0	X	X	X	0	0	0	0	0	5x7 Dots 1 Character 	Alphanumeric mode
②	1	0	1	X	X	X	0	0	0	0	0	8x12 Dots 1 Character External ROM Code 	Alphanumeric mode
③	1	0	1	0	X	X	X	X	X	X	64x32 display elements 4 Dots 	Semigraphics 4 mode	
④	1	0	1	1	X	X	X	X	X	X	64x48 display elements 4 Dots 	Semigraphics 6 mode	
⑤	1	1	X	X	0	0	0	0	X	0	64x64 display elements 2 Dots 	Color graphic mode 64x64	
⑥	1	1	X	X	0	0	1	0	X	0	128x84 display elements 2 Dots 	Graphic mode 128x64	
⑦	1	1	X	X	0	1	0	1	X	0	128x64 display elements 2 Dots 	Graphic mode 128x64	
⑧	1	1	X	X	0	1	1	0	X	0	128x96 display elements 2 Dots 	Graphic mode 128x96	
⑨	1	1	X	X	1	0	0	1	X	0	128x96 display elements 2 Dots 	Color graphic mode 128x96	
⑩	1	1	X	X	1	0	1	0	X	0	128x192 display elements 2 Dots 	Graphic mode 128x192	
⑪	1	1	X	X	1	1	0	1	X	0	128x192 display elements 2 Dots 	Color graphic mode 128x192	
⑫	1	1	X	X	1	1	1	1	X	0	256x192 display elements 1 Dot 	Graphic mode 256x192	

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Internal Character Generator

The M5C6847P-1 generates the 64 standard ASCII characters in a 5 x 7 dot matrix form. It generates the 64 standard ASCII characters according to a 6-bit code. The code for each character is showed in Table 5.

EXAMPLE OF DISPLAY ON CRT

The M5C6847P-1 can be used to generate characters for display on a video screen. An example of a display is shown in Fig. 1.

Table 5 M5C6847P-1 character set

Code						Character	Code						Character
D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
0	0	0	0	0	0	@	1	0	0	0	0	0	SP
0	0	0	0	0	1	A	1	0	0	0	0	1	!
0	0	0	0	1	0	B	1	0	0	0	1	0	"
0	0	0	0	1	1	C	1	0	0	0	1	1	#
0	0	0	1	0	0	D	1	0	0	1	0	0	\$
0	0	0	1	0	1	E	1	0	0	1	0	1	%
0	0	0	1	1	0	F	1	0	0	1	0	1	&
0	0	0	1	1	1	G	1	0	0	1	1	0	.
0	0	1	0	0	0	H	1	0	1	0	0	0	(
0	0	1	0	0	1	I	1	0	1	0	0	1)
0	0	1	0	1	0	J	1	0	1	0	1	0	*
0	0	1	0	1	1	K	1	0	1	0	1	1	+
0	0	1	1	0	0	L	1	0	1	1	0	0	=
0	0	1	1	0	1	M	1	0	1	1	0	1	-
0	0	1	1	1	0	N	1	0	1	1	1	0	.
0	0	1	1	1	1	O	1	0	1	1	1	1	/
0	1	0	0	0	0	P	1	1	0	0	0	0	0
0	1	0	0	0	1	Q	1	1	0	0	0	1	1
0	1	0	0	1	0	R	1	1	0	0	1	0	2
0	1	0	0	1	1	S	1	1	0	0	1	1	3
0	1	0	1	0	0	T	1	1	0	1	0	0	4
0	1	0	1	0	1	U	1	1	0	1	0	1	5
0	1	0	1	1	0	V	1	1	0	1	1	0	6
0	1	0	1	1	1	W	1	1	0	1	1	1	7
0	1	1	0	0	0	X	1	1	1	0	0	0	8
0	1	1	0	0	1	Y	1	1	1	0	0	1	9
0	1	1	0	1	0	Z	1	1	1	0	1	0	:
0	1	1	0	1	1	[1	1	1	0	1	1	:
0	1	1	1	0	0	\	1	1	1	1	0	0	<
0	1	1	1	0	1]	1	1	1	1	0	1	=
0	1	1	1	1	0	↑	1	1	1	1	1	0	>
0	1	1	1	1	1	←	1	1	1	1	1	1	?

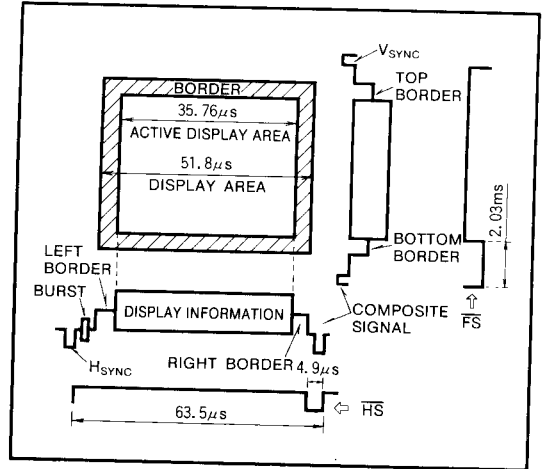


Fig. 1 Example of a display by a M5C6847P-1

APPLICATION EXAMPLES

One example of interfacing a M5C6847P-1 with a television set for home use is shown in Fig. 2. A M5L8085AP is used as the CPU in the example shown. The CPU executes the programs to control display and write the information for one screen into display memory. The M5C6847P-1 performs the main functions of interfacing with the CRT such as synchronizing scan, reading the display information from the display memory while adding necessary synchronization signals and sending to the RF modulator.

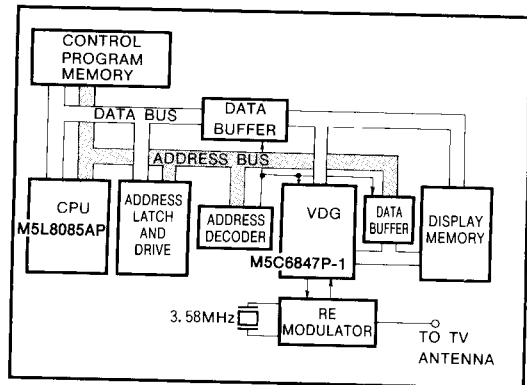


Fig. 2 Application example using the M5C6847P-1

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A schematic for using the M5C6847P-1 with the M51342P RF modulator is shown in Fig. 3. M51342 requires $\pm 5V$ power supplies. The video signal and chroma signal from the M5C6847P-1 can be modulated with the sound signal to form a RF signal that appears the same as the television antenna input signal. The video amplifier circuit to enable direct con-

nection to a M5C6847P-1 is shown in Fig. 4. This can be connected to the monochrome video monitor. In this case, the impedance is 75Ω .

Four levels of brightness (black, low, medium and high) can display a clear picture.

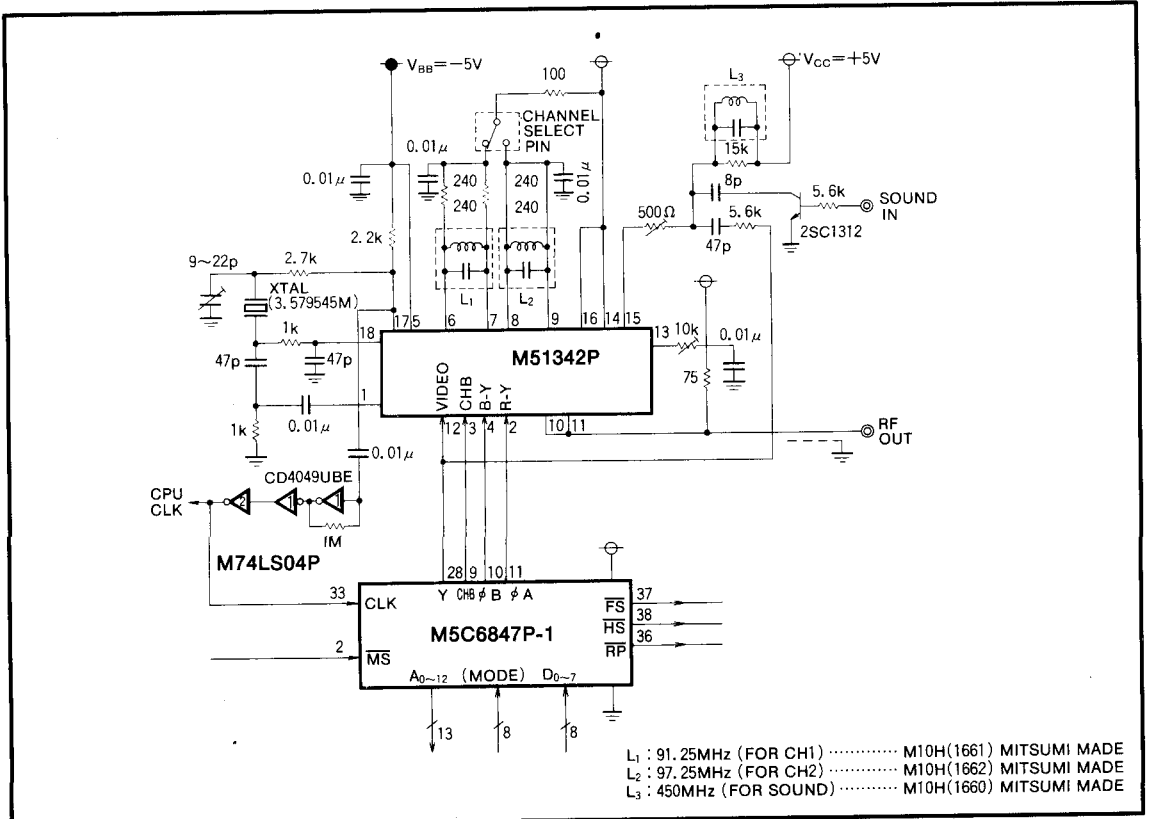


Fig. 3 Schematic for using the M51342P (RF modulator) with the M5C6847P-1

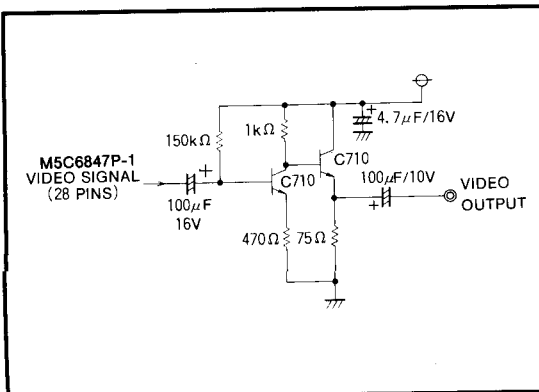


Fig. 4 Video amplifier circuit

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Data and Display Relation

The relation between data and 5 display modes is shown in Table 6.

Table 6 Data and display relation

Mode	Data	Display
Character	<p>D7 D6 D5 D4 D3 D2 D1 D0 6-bit ASCII</p>	<p>5 dots Height 12 dots 7 dots Width 8 dots</p>
Semigraphic 4	<p>D7 D6 D5 D4 D3 D2 D1 D0 Color designation Display element ON/OFF indication</p>	<p>D1 D0 D2 D3 — Display element</p>
Semigraphic 6	<p>D7 D6 D5 D4 D3 D2 D1 D0 Color designation Display element ON/OFF indication</p>	<p>D1 D0 D3 D2 D5 D4 — Display element</p>
Color-graphic (4 colors)	<p>D7 D6 D5 D4 D3 D2 D1 D0 Color designation Color designation Color designation Color designation</p>	<p>Display element</p>
Graphic (2 colors)	<p>D7 D6 D5 D4 D3 D2 D1 D0 Display element ON/OFF indication</p>	<p>Display element</p>

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		-0.3~7	V
V_I	Input voltage	With respect to V_{SS}	-0.3~7	V
V_O	Output voltage		-0.3~7	V
P_d	Power dissipation	$T_a=25^\circ\text{C}$	1000	mW
T_{opr}	Operating free-air temperature range		0~70	$^\circ\text{C}$
T_{stg}	Storage temperature range		-65~150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a=0\sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
$V_{IH(\phi)}$	High-level input voltage, clock	2.4		V_{CC}	V
V_{IH}	High-level input voltage	2		V_{CC}	V
$V_{IL(\phi)}$	Low-level input voltage, clock	-0.3		0.4	V
V_{IL}	Low-level input voltage	-0.3		0.8	V

ELECTRICAL CHARACTERISTICS ($T_a=0\sim 70^\circ\text{C}$, $V_{CC}=5V\pm 5\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage, except for ϕA , ϕB , Y, and CHB output	$V_{SS}=0V$, $I_{OH}=-100\mu\text{A}$, $C_L=30\text{pF}$	2.4			V
V_{OL}	Low-level output voltage, except for ϕA , ϕB , Y and CHB output	$V_{SS}=0V$, $I_{OL}=1.6\text{mA}$, $C_L=30\text{pF}$			0.4	V
I_{IH}	High-level input current	$V_{SS}=0V$, $V_I=5.25V$	-10		10	μA
I_{IL}	Low-level input current	$V_{SS}=0V$, $V_I=0V$	-10		10	μA
I_{OZ}	Output floating leak current	$V_{SS}=0V$, $V_I=0.4V$, $MS=0.4V$	-10		10	μA
I_{CC}	Supply current from V_{CC}	$V_{SS}=0V$			150	mA
C_i	Input capacitance	$V_I=0V$, $f=1\text{MHz}$, $T_a=25^\circ\text{C}$			10	pF
C_O	Output capacitance				20	pF
V_{CHB}	Chroma bias voltage			0.6 V_{CC}		V
$V_{\phi A,H}$	ϕA chrominance high-level output voltage			$V_{CHB}+$ 0.16 V_{CC}		V
$V_{\phi A,M}$	ϕA chrominance medium-level output voltage			V_{CHB}		V
$V_{\phi A,L}$	ϕA chrominance low-level output voltage			$V_{CHB}-$ 0.16 V_{CC}		V
$V_{\phi B,H}$	ϕB chrominance high-level output voltage			$V_{CHB}+$ 0.16 V_{CC}		V
$V_{\phi B,M}$	ϕB chrominance medium-level output voltage			V_{CHB}		V
$V_{\phi B,B}$	ϕB chrominance burst-level output voltage			$V_{CHB}-$ 0.08 V_{CC}		V
$V_{\phi B,L}$	ϕB chrominance low-level output voltage	$V_{SS}=0V$, $C_L=20\text{pF}$, $R_L=200\text{k}\Omega$		$V_{CHB}-$ 0.16 V_{CC}		V
V_{YSYNC}	Luminance sync output voltage			0.74 V_{CC}		V
V_{YBLANK}	Luminance blank output voltage			0.85 V_{YSYNC}		V
V_{YBLACK}	Luminance black output voltage			0.81 V_{YSYNC}		V
$V_{YW(H)}$	White luminance high-level output voltage			0.62 V_{YSYNC}		V
$V_{YW(M)}$	White luminance medium-level output voltage			0.69 V_{YSYNC}		V
$V_{YW(L)}$	White luminance low-level output voltage			0.77 V_{YSYNC}		V

VIDEO DISPLAY GENERATOR

TIMING REQUIREMENTS ($T_a=0\sim 70^\circ\text{C}$, $V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$f_C(\phi)$	Clock frequency		3.579535	3.579545	3.579555	MHz
f_{DUTY}	Clock duty ratio		45	50	55	%
$t_r(\phi)$	Clock rise time				30	ns
$t_f(\phi)$	Clock fall time				30	ns
$t_{a(A-D)I}$	Address access time of display memory	Internal character mode			900	ns
$t_{a(A-D)E}$	Address access time of display memory + Address access time of external character ROM	External character mode			900	ns

SWITCHING CHARACTERISTICS

Composite video and chroma ($T_a=0\sim 70^\circ\text{C}$, $V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_w(YSYNC)$	Luminance output synchronization signal pulse width			4.89		μs
$t_w(YFP)$	Luminance output front porch signal pulse width			1.96		μs
$t_w(YHBLANK)$	Luminance output horizontal blank signal pulse width			11.73		μs
$t_r(YHSYNC)$	Luminance output horizontal synchronization signal rise time				250	ns
$t_f(YHSYNC)$	Luminance output horizontal synchronization signal fall time				250	ns
$t_r(YHBLANK)$	Luminance output horizontal blank signal rise time				340	ns
$t_f(YHBLANK)$	Luminance output horizontal blank signal fall time				340	ns

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CHROMA

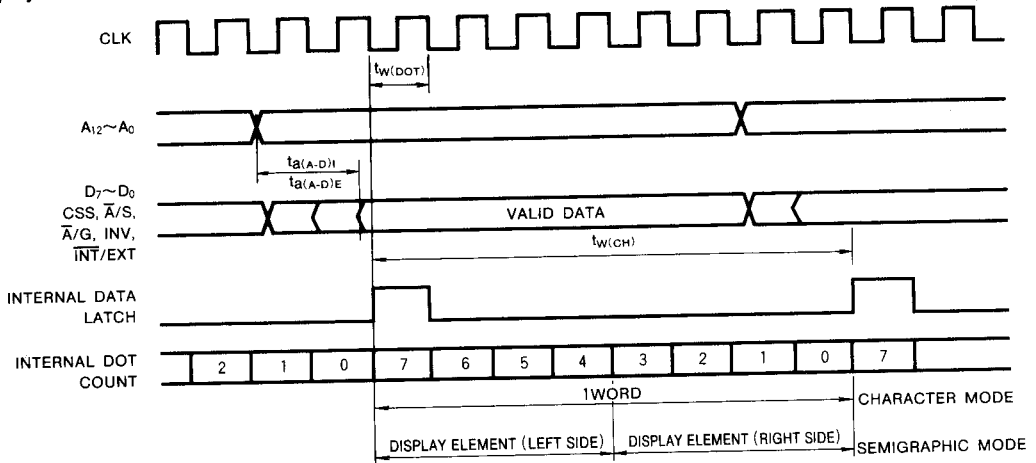
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_r(\phi A)$	ϕA chrominance output rise time			60		ns
$t_f(\phi A)$	ϕA chrominance output fall time			60		ns
$t_r(\phi B)$	ϕB chrominance output rise time			60		ns
$t_f(\phi B)$	ϕB chrominance output fall time			60		ns
$t_{PHL}(SYNC-BURST)$	ϕB chrominance output propagation time after luminance synchronization signal output			980		ns
$t_w(BURST)$	ϕB chrominance output burst signal pulse width			2.93		μs
$t_r(BURST)$	ϕB chrominance output burst signal rise time			60		ns
$t_f(BURST)$	ϕB chrominance output burst signal fall time			60		ns
$t_{PHL}(Y-CH)$	Chrominance propagation time after luminance output			0		ns

MISCELLANEOUS

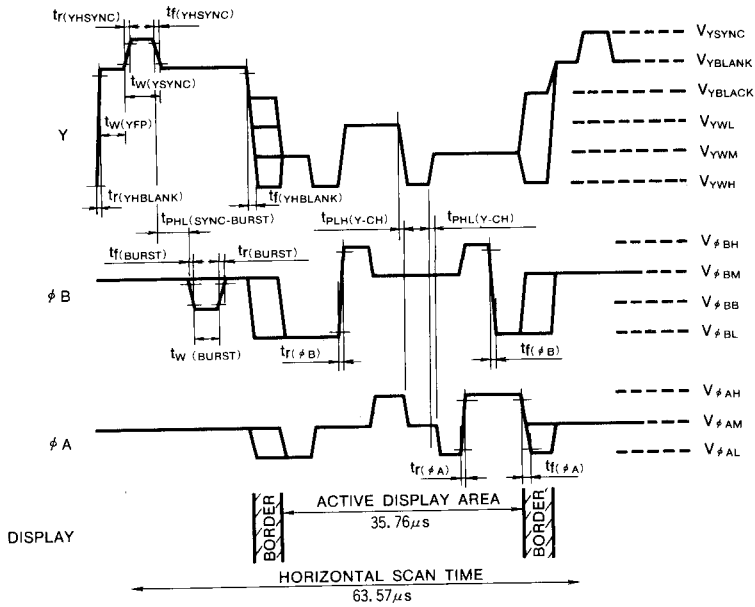
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_w(FS)$	Field synchronization pulse width			2.03		ms
$t_w(RP)$	Row preset pulse width			980		ns
$t_{PHL}(HS-RP)$	RP propagation time after HS			980		ns
$t_w(HS)$	Horizontal synchronization pulse width			4.9		μs
$t_w(CH)$	Character width			1.12		μs
$t_w(DOT)$	Dot width			140		ns

TIMING DIAGRAM

Display memory access



Composite video and chroma



Miscellaneous timing

